AMENDMENTS TO THE SPECIFICATION

Page 1, lines 8-9 should be amended as follows:

This is a continuation-in-part of U.S. Patent ~~Application Serial~~ No. ~~09/102,740 filed June 22, 1998~~ 6,289,068 B1 which issued on September 11, 2001.

B1

Page 1, lines 13-16 should be amended as follows:

This application relates to commonly assigned ~~Application Serial No. 09/102,704~~ U.S. Patent No. 6,400,735 B1 which issued on June 4, 2002, entitled "Glitchless Delay Line Using Gray Code Multiplexer", which is incorporated herein by reference.

B2

Page 13, lines 20-31 should be amended as follows:

Within delay lock loop 300, reference clock signal REF_CLK is delayed by delay line 310 to generate delayed clock signal D_CLK. Delayed clock signal D_CLK is delayed from clock signal REF_CLK by a propagation delay D in delay line 310. One embodiment of delay lock loop 300 uses an adjustable delay line described in U.S. ~~Application Serial No. 09/102,704 [docket X-440 US]~~ Patent No. 6,400,735 B1, entitled "Glitchless Delay Line Using Gray Code Multiplexer", which is referenced above. However, other adjustable delay lines can also be used with delay lock loop 300. Delayed clock signal D_CLK is provided to an input terminal of a clock phase shifter 350 and to an input terminal of an output generator 340.

B3

Page 45, lines 9-23 should be amended as follows:

After delay lock loop 400 becomes locked, the ~~DLLS_LOCKED~~ DLL_LOCKED signal transitions to a logic high value. In response, NAND gate 1809 provides a logic "0" output signal. This logic "0" signal is latched into flip-flop 1805 on the next rising edge of the PS_DLY_OUT signal. As a result, OR gate 1808 provides a logic "0" signal which releases pattern generator 1801, 5-bit up counter 1804 and flip-flop 1805. At this time, pattern generator 1801 is enabled to generate a predetermined

B4 Cont

pattern. The particular pattern is selected by the SPREADSEL[3:0] signal. In one embodiment, pattern generator 1801 is capable of generating patterns for creating spread-2, spread-4, spread-6, spread-8, spread-16, spread-32, and spread-64 configurations. In the present example, the SPREADSEL[3:0] signal is selected to provide a pattern for a spread-8 configuration.

B4 cont

Page 47, lines 30-36 through page 48, lines 1-7 should be amended as follows:

During the fourth clock cycle C4, pattern generator 1801 is enabled and provides a trim signal t[9:0] having a value equal to 2 trim settings. In response, signed adder circuit 1802 ~~provides~~ adds two trim settings to the PS_TT[8:0] signal provided by up/down counter 1311. As a result, the cycle C4 of the S_CLK signal is lengthened by two trim settings, or 100 ps. Cycle C4 of the S_CLK signal therefore has a period of 10100 ns, such that the rising edge of the fifth cycle C5 of the S_CLK signal occurs at 40100 ns. At this time, there is an initial offset of 100 ns between the REF_CLK and S_CLK signals. This initial offset is provided one time only before implementing the normal spread-8 configuration. This initial offset enables the spread 8 configuration to be implemented in an optimal manner as described below.

B5

Please amend the Abstract as follows:

The frequency of a skew clock signal is dithered around a base frequency, thereby enabling this clock signal to comply with FCC requirements for electromagnetic emissions within a specified window ~~(e.g., a 1 MHz window)~~. ~~That is, delay can be~~ Delay is introduced such that the clock signal~~s~~ exhibit~~s~~ slightly different frequencies in successive periods. For example, the frequency of a 100 MHz clock signal can be adjusted to have frequencies of approximately 98, 98.5, 99, 99.5, 100, 100.5, 101, 101.5, and 102 MHz during different periods. ~~This configuration is referred to as a spread-8 configuration,~~

B6 cont

~~because eight frequencies are used in addition to the base frequency of 100 MHz.~~ Because the frequencies are spread in 0.5 MHz increments, only three ~~of the nine~~ frequencies are included in any 1 MHz window. As a result, 2/3 of the energy of the clock signal is not included when determining whether the clock signal meets the FCC electromagnetic emission requirements ~~in this test~~. By spreading the frequencies above and below the base frequency in a regular manner, the average frequency of the clock signal becomes equal to the base frequency. ~~Other configurations including, but not limited to, spread-2, spread-4, spread-6, spread-16 and spread-32 configurations, can also be implemented.~~

BK cont'd